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A Computer Interface for a Perkin-Elmer
5000 Atomic Absorption Instrument

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A COMPUTER INTERFACE FOR A PERKIN-ELMER 5000
ATOMIC ABSORPTION INSTRUMENT

by
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FOREWORD

Environmental measurements are required to determine the quality of ambient waters and the character of waste effluents. The Environmental Monitoring and Support Laboratory - Cincinnati, conducts research to:

- Develop and evaluate techniques to measure the presence and concentration of physical, chemical, and radiological pollutants in water, wastewater, bottom sediments, and solid waste.
- Investigate methods for the concentration, recovery, and identification of viruses, bacteria and other microbiological organisms in water; and to determine the responses of aquatic organisms to water quality.
- Develop and operate an Agency-wide quality assurance program to assure standardization and quality control of systems for monitoring water and wastewater.
- Develop and operate a computerized system for instrument automation leading to improved data collection, analysis, and quality control.

This report was developed in the Advanced Instrumentation Section of the Environmental Monitoring and Support Laboratory in the interest of advancing laboratory techniques and quality control through computerization.

Robert L. Booth

Robert L. Booth
Acting Director
Environmental Monitoring and Support
Laboratory - Cincinnati

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ABSTRACT

This document contains a detailed description of an ASCII Character Buffer Interface designed to store and forward serial ASCII data received from an EIA RS-232C Interface. The particular application described herein concerns a Perkin Elmer Model 5000 Atomic Absorption instrument transmitting ASCII data to the Data General EPA Laboratory Automation System.

The interface is a part of a larger atomic absorption computer automation system which is currently in operation at the Environmental Protection Agency, Environmental Monitoring and Support Laboratory-Cincinnati. Software has been developed¹ on the multi-user Basic language system for atomic absorption instrument applications. Applications include "on line" data reduction, quality control, report generation and sample file control. The interface, however, may be used in any application involving the need to store and forward ASCII information.

This report covers a period from December 1979 to January 1980 and work was completed as of January 1980.

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CONTENTS

Foreword.....	iii
Abstract.....	iv
Figures.....	vi
Tables.....	vi
Abbreviations and Symbols.....	vii
1. Introduction.....	1
2. Conclusion.....	2
3. Design Objectives.....	3
4. Functional Design of the Complete Interface System.....	4
5. Functional Design of the ACB Interface.....	5
EIA interface compatibility.....	5
Memory requirements.....	5
Pseudo real/time data acquisition.....	6
6. Functional Design of the NOVA Interface.....	7
7. Circuit Description of the ACB Interface.....	8
8. Circuit Description of the NOVA Interface.....	11
9. Cost and Fabrication.....	13
References.....	14
Appendices	
A. EIA Modem -Terminal interface.....	29
B. Perkin-Elmer 5000 EIA RS-232C interface description.....	30
C. Assembly code interface to the NOVA.....	31

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HERE

FIGURES

Number

Page

1	ACB interface block diagram.....	19
2	UART Call 40 flowchart.....	20
3	NOVA interface block diagram.....	21
4	NOVA interface schematic diagram.....	22
5	ACB interface schematic diagram.....	23
6	The ACB write function synchrogram.....	24
7	The ACB send function synchrogram.....	25
8	Parts layout for ACB interface (mother board).....	26
9	Parts layout for Memory Card.....	27
10	Parts layout for NOVA inteface.....	28

TABLES

Number

Page

1	Parts list for ACB interface (mother board).....	15
2	Parts list for ACB interface (memory card).....	16
3	Parts list for NOVA interface.....	17
4	Parts list for ACB interface (Enclosure).....	18

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LIST OF ABBREVIATIONS AND SYMBOLS

ABBREVIATIONS

ACB	-- ASCII character buffer
ASCII	-- American Standard Code for Information Interchange
CE	-- chip enable
DO	-- data out
FIFO	-- first in first out
FLOP	-- flip-flop
II	-- intelligent instrument
PE 5000	-- Perkin Elmer model 5000 atomic absorption instrument
PC	-- printed circuit
NOVA	-- The Data General EPA Laboratory Automation System
RDA	-- read data available, pin 19 on a UART chip
RDAR	-- read data available reset, pin 18 on a UART chip
RSI	-- receive serial input, pin 20 on a UART chip
RTS	-- request to send, pin 4 on a EIA RS-232C interface
TBMT	-- transmit buffer empty, pin 22 on a UART chip
TDS	-- transmit data strobe, pin 23 on a UART chip
UART	-- universal asynchronous receiver/transmitter

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SECTION 1

INTRODUCTION

With the advent of intelligent instruments (II) in the analytical laboratory, the need for transferring data between them and more powerful computer systems becomes increasingly apparent. Intelligent instruments are defined in this report as any instrument with the capability to output serial ASCII information. Usually, this ASCII information is transmitted via a standard EIA RS-232C interface (See Appendix A). Normally, the minicomputer/microprocessor within the intelligent instrument does not support a full handshake operation in the EIA RS-232C interface. That is, there are neither "clear to send, pin 5" or "request to send, pin 4" signals in the II's EIA RS-232C interface. The signals are usually hardwired to a fixed voltage level (See Appendix B). By hardwiring the signals, the II presumes that the receiving system is always ready to receive characters transmitted from the II. The receiving system is specifically the Data General 840 NOVA laboratory automation system² in this application and will hereafter be referred to as the NOVA.

This presumption poses problems for some multi-user computer systems which may not have the ability to dedicate memory to the buffering of characters from the II or the dedication of a hardware serial ASCII port to the characters coming from the II may not be practical. In any event, the need to store and forward ASCII information from II utilizing a handshake approach becomes desirable. Since nothing cost beneficial was available from commercial sources, for solving the above dilemma, an interface was designed "in-house."

The ASCII character buffer (ACB) interface is proposed to provide a means to receive data from an EIA RS-232C interface, to store the information in memory circuits, check the NOVA to verify readiness to accept data, and to send the stored information to the NOVA in a first-in first-out (FIFO) mode of operation. Transmission would be accomplished on a character by character basis with handshake controls passing between the NOVA and the ACB interface.

The NOVA, upon receiving the transmitted character, would have the ability to prevent further transmissions of data by dropping the "request to send" signal in the RS-232C interface. To receive additional characters from the ACB interface the NOVA would merely send the request to send flag to the ACB interface, and the ACB interface would respond by transmitting another character to the NOVA.

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CONCLUSIONS

The ACB interface provides a link between the Perkin Elmer Model 5000 atomic absorption instrument (PE 5000) and the EPA Data General NOVA Laboratory Automation system operating in a multi-user basic language real/time data acquisition and reduction mode. The ACB interface takes advantage of the distributed processing in the PE 5000 instrument. And at the same time the interface marries the PE 5000 to the Data General laboratory automation system for "on line" data acquisition, data reduction and quality assurance.

This link was designed for general purpose applications. Any EIA RS-232C interface can be used for input or output from the interface. For example, the new Technicon autoanalyzer model II C upgrades could be interfaced to the EPA laboratory automation system using the ACB interface and the universal asynchronous receiver/transmitter (UART) interface in the NOVA. For IIs with the "request to send" flag enabled in the RS-232C interface, a direct connection can be made to the UART interface with NOVA. This would eliminate the ACB interface due to the handshake capability already present.

Together the two modules (ACB interface and NOVA Interface) provide a general purpose solution to II interfaces which are low volume transmissions yet which need immediate attention.

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SECTION 3

DESIGN OBJECTIVES

- The serial ASCII information must be transferred in a first-in first-out (FIFO) basis.
- Transmission of the ASCII information must operate in a "handshake mode." That is, ready flags must be queried before characters are transmitted.
- The interface must have the capability to receive information at any time.
- The interface must be able to buffer all characters received without losing any information.
- The interface must have capability of transferring information at speeds that are reasonably close to real/time, that is so the operator of the instrument may use processed information to make decisions about the quality of current data.

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SECTION 4

FUNCTIONAL DESIGN OF THE COMPLETE INTERFACE SYSTEM

The complete interface system for the PE 5000 consists of two independent hardware modules: an ACB interface module and a NOVA interface module. The module designated ACB interface is responsible for receiving and storing serial ASCII information coming from the PE 5000 interface. This module will store the information in memory circuits and query to "Request to Send" (RTS) flag of the EIA interface connected to the NOVA. If the RTS flag is "true", information will be sent to the NOVA. This handshake mode of data transmission will prevent any information from being lost.

The ACB interface was designed for compatibility with any EIA or RS-232C interface. The module is therefore compatible with practically any computer system in the field today. This was intentionally done to allow flexibility in the buffering of the PE 5000's data. The ACB interface will allow data from the PE 5000 to be transmitted to any type of computer automation system with an RS-232C interface operating in a handshake mode.

The module designated NOVA interface is responsible for receiving the information at the NOVA. The NOVA computer does not have the capability to receive RS-232C data in a handshake fashion. The NOVA interface provided this handshake function. As soon as a character is detected at the NOVA, the NOVA interface will stop further transmission by dropping the RTS flag in the RS-232C interface. When the serial ASCII character is read into the memory of the NOVA, the NOVA interface is reset to allow another character to be received.

This design allowed the NOVA to accept serial ASCII data in a handshake fashion. Not only can this design be applied to the ACB interface at the PE 5000, but any instrument system capable of RS-232C handshake communication can now be interfaced to the NOVA provided the RTS flag is present.

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PSEUDO REAL/TIME DATA ACQUISITION

In this particular application involving the PE 5000 the data from the 5000 are required by the NOVA as soon as possible. The ACB interface will begin communicating the ASCII information to the NOVA as soon as the first character is received.

The three criteria which must be present before the ACB interface will transmit a character are:

- The receive counter must contain more counts than the send counter;
- The NOVA must be ready to receive a character (The "request to send flag" is true from the NOVA); and
- The UART in the ACB interface must be ready to transmit another character (Transmit Buffer Empty TBMT is true on the UART).

The ACB interface has the capability to receive information at 30 characters per second (300 baud). This baud rate is totally a function of the receive clock fed into the UART in the ACB interface. For the PE 5000 application, both clocks were set at the 300 baud rate. However, only the UART transmit or receive clock need be changed to alter the transmit or receive baud rate.

The hardware/software interface at the Nova has the capability to input a maximum of 7.5 characters per second; therefore, the 30 character per second rate (300 baud) was more than sufficient to meet the NOVA interface needs. Since only seventeen characters are being transmitted per injection from the PE 5000, this will require approximately 2.5 seconds for all the information from a single furnace atomic absorption injection to be received by the NOVA. Since injections are normally spaced approximately two minutes apart, 2.5 seconds is a reasonable amount of time to allow for data transmission.

This mode of data transfer will allow the analyst at the PE 5000 to have calculated concentrations and quality assurance data displayed at the user NOVA terminal within a few seconds after the absorbance data were produced by the PE 5000. That is, the Basic language application program is programmed to immediately accept data from the NOVA interface and perform the necessary calculations, report the quality assurance data, and output results to the operator.

SECTION 6

FUNCTIONAL DESIGN OF THE NOVA INTERFACE

The NOVA interface can be divided into two main sections: hardware and the software. The hardware section has the capability to receive a serial ASCII transmission from an RS-232C interface. As soon as a serial ASCII character is sensed (at the first "mark" pulse), the hardware section drops the RTS flag of the RS-232C interface. Upon reception of the complete ASCII character, the hardware raises an appropriate "done" flag to signal the software that the character is available for input into an accumulator. The character at this time has been converted from a serial string of data into a set of parallel data which are connected to the input of multiplexer #2 on the NOVA digital input chassis.

After the software has read the information into the accumulator, the hardware section can be reset to allow another character to be received. Figure 3 illustrates the block diagram of the hardware section.

The NOVA software section has the capability to read 8 bits of information (UART received data) into the basic language as a variable. The data are read into the BASIC language via a CALL 40, A (A is the variable which has the decimal equivalent of the ASCII character returned from the CALL). The listings to CALL 40 are contained in Appendix C. There is reference material available for additional information on real/time calls implemented on a Data General 840 in Basic.³

Once a user program executes a CALL 40 subroutine, it will remain in that subroutine until the UART in the digital bay receives a character and sets the done flag or until the escape key is pressed. The UART in the digital bay has the ability to be reset by an octal instruction 62467. The instruction which reads multiplexer two in the digital bay is 61460. The flowchart for the CALL 40 is shown in Figure 2.

After the character is read into BASIC, the UART flag RDAR (Figure 3) is automatically reset to allow another character to be received.

The schematic for the UART in the digital bay is shown in Figure 4 and will be described in the NOVA interface circuit description section.

The NOVA interface was designed for general purpose application. Any instrument capable of EIA RS-232C data transfer which has the RTS flag enabled will be able to transfer data to the NOVA without the need for any external circuitry, such as the ACB interface.

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SECTION 5

FUNCTIONAL DESIGN OF THE ACB INTERFACE

EIA INTERFACE COMPATIBILITY

EIA driver circuits and EIA receiver circuits will be used to communicate into and out of the ACB interface (See Figure 1). This will provide hardware compatibility with any type of device utilizing an EIA RS-232C interface. Any II can feed information into the ACB interface and the information will be transmitted to any computer system with an EIA RS-232C interface.

MEMORY REQUIREMENTS

The FIFO memory storage is accomplished by two counters which will address the memory. The receive counter incorporated in the ACB interface will count the number of characters received from an II. The send counter will cause transmission of characters from memory until its count matches the receive counter's count. In each case as the function is performed, the appropriate counter is incremented and the corresponding count is used to address the memory. The send counter's address is always following the receive counter's address around the 1000 words of memory.

A limitation which is readily apparent is the overlap of memory. In this interface design, 1000 characters can be stored and forwarded until the counters write over themselves. Since the Perkin Elmer Model 5000 Atomic Absorption Instrument (PE 5000) transmits 17 characters per sample and there are 40 positions in the sample tray, the above character storage will allow data from a full tray of samples to be stored ($17 \times 40 = 680$).

The interface was designed, however, in such a fashion that up to 4000 characters can be accommodated with minor circuit changes. The counters used in the design are 12 bit binary counters of which only 10 bits are presently being used in the PE 5000 interface design. Even the comparators used to determine when the receive counter matches the send counter have the capability for 12 bit operation. A memory board was designed to plug into the mother board so that if additional memory should ever be required the modification can be made on the memory card as opposed to the motherboard. Therefore, only the additional address lines need to be brought over to the memory board connector if additional memory is required.

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CIRCUIT DESCRIPTION OF THE ACB INTERFACE

Figure 5 illustrates the complete schematic of the ACB interface. As ASCII data are received from the Cinch DB-25P EIA RS-232C standard connector, U19 converts the RS 232C level signals to TTL level signals for input into the U22 (Com 2017 Universal Asynchronous Receiver Transmitter (UART) Chip). The serial ASCII TTL data are fed into the receive serial input (RSI) of the UART chip. When the received information is ready to be read out of the received data buffer, the read data available (RDA) flag on the UART chip goes high.

THE WRITE FUNCTION

This RDA flag is the D input of the U1 D flip-flop (flop). With the D input true, the next positive going clock pulse from pin 3 of U11 causes the D information to be transferred to the Q output of U1 (Pin 1); Q bar will be on U1 Pin 2.

The two flops on the U1 chip control the two main functions of the ACB interface. The flop with the D input on pin 5 will write data received by the UART chip into memory. The flop with the D input on pin 9 will read data from memory and cause the transmission of data by the UART chip. The two flops can never be in operation at the same time. When one flop is in operation, it prevents the other flop from receiving the clock pulse by dropping one of the inputs to the AND gates feeding the clocks to the flops. For instance, as the write flop is activated, Q bar is fed into pin 6 of U11 thereby preventing any further clock pulses from getting to the send flop. Even if the send flop's D input is high, this information is prevented from getting through the flop by the prevention of the clock pulse coming from pin 4 of U11. Similarly, if the send flop is activated, the write flop is prevented from operation by driving pin 2 of U11 low by the Q bar output of the send flop. This either/or action is necessary due to the memory access function needed by the ACB interface. That is, the two functions can never access memory at the same time.

Therefore, as the write flop's Q outputs are activated, Q bar immediately enables the data from the receive buffer on the UART to be fed into the data in pins of the memory chips. This is accomplished by tying the Q bar output to the read data enable (RDE) pin 4 on the UART chip. Since the Q bar also clocks the binary counter U2, the write memory pulse coming from Pin 3 of U16 is prevented until the negative going transition of the clock takes place. This is accomplished by the clock inversion at U10 pin 4 nanded with the Q output of U1 pin 1. See the Synchrogram in Figure 6.

The reason for delaying the write pulse is due to the settling time of the binary counters (U2 and U18), which require approximately 7.5 micro-seconds to settle. Therefore, the positive going edge of the clock pulse has to be a minimum of 8 micro-seconds wide. Since the 300 baud ($300 \times 16 = 4800$ Hz) clock feeding the UART from U18 has an approximate positive pulse width of 104 microseconds, the UART clock was used to clock the flops also. The 208 microsecond clock will easily allow up to a 4800 baud operation of the UART.

Q bar of the write flop also enables the tri-state buffers of the U2 binary counter. This is the memory address where the data are to be written. Q bar of the write flop causes pin 4 of U16 to go high which causes Pin 2 of U10 to go low thereby chip enabling (CE) the memory of the interface. Notice that CE is active when either Q bar from the flops is low by means of the nand gate U16 pin 6 or 5.

The write flop immediately supplies the CE pulse, enables the addressing of the memory, increments the U2 binary counter and enables one half of the nand gate U16 at pin 2. As the clock goes low pin 3 of U16 writes the information into the memory at the address of the binary counter U2. Pin 3 of U16 also activates the one shot on U12 by driving pin 5 of U12 low. The time to write the received data on the UART into memory takes approximately 200 nanoseconds. The time required by the one shot on U12 to get the information to its Q and Q bar outputs takes approximately one microsecond with an external timing capacitor of 100 PF. Therefore, by the time the one shot fires (set for a 1 microsecond pulse width) the data are already written into the memory. Therefore, as Q pin 6 of U12 resets the write flop U1 at pin 4 the data are already stored in memory. Q bar of the one shot pin 7 resets the read data available reset (RDAR) pin 18 of the UART. Thereby allowing the UART to be available for receiving the next serial ASCII character.

THE TRANSMIT FUNCTION

The comparators, U13, U14, and U15, compare the addresses of the binary counters U2 and U18. If the binary counters are not equal, pin 3 of U13 goes low and stays low until the receive counter (U2) and the send counter (U18) are equal. The equal flag from U13 pin 3 is inverted by U10 inverter (9, 10) and fed into the AND gate of U11 pin 13. This equal flag is one of three inputs which must be true before the send flop is activated. The transmit buffer empty flag must also be present from the UART pin 22 (TBMT). This flag is fed into U11 pin 12. With the equal flag present and the TBMT flag present U11 pin 11 is then true to U11 pin 9. The third flag which must be present is the "Request to Send" flag from the RS 232C interface-pin 4 of the "To NOVA" connector. The RS 232C signal is converted to a CMOS level by means of the EIA receiver U19 driver 4,6. The output of U19 pin 6 is fed into the U11 pin 8 and gate which outputs a true to the D input of the send flop if there is a true from U11 pin 11.

The send flop will be activated on the next positive going transition of the clock by means of the AND gate U11 pin 4, provided it is not locked out by the activation of the write flop. The send flop immediately increments

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the send counter by the negative going pulse from Q bar on U1 pin 12 being fed into the binary counter U18 pin 10. Again the CE is also enabled by the Q bar of U1 pin 12 being fed into the U15 pin 5 input to the nand gate controlling the CE signal. Q bar of U1 pin 12 also locks out the write flop by dropping the input to the AND gate U11 pin 2 which disables the clock to the write flop.

Q bar of the transmit flop enables the address lines of the tri-state buffers, buffering the address from the send binary counter U18. Again a positive going clock pulse delay is necessary to allow for the settling of the U13 binary counter. This is accomplished by a U19 inverter 7,6 and the nand gate U16 with inputs on pins 8 and 9.

Upon the negative going transition of the clock pulse U16 pin 10 supplies a transmit data strobe (TDS) to the UART which begins the transmission of the information read from the memory addressed by the counter U18. The TDS signal has a minimum width of 200 nanoseconds. Besides supplying the TDS signal, the U16 pin 10 activates the other half of the U12 one shot multivibrator. Again the Q outputs of the one shot will be delayed a minimum of 750 nanoseconds from the time pin 11 of U12 is activated until the Q and Q bar outputs respond. This is more than enough time for the TDS signal to the UART to have enabled the transmission of the data fed into the transmit buffer from the data out (DO) outputs of the memory. See the Send Function Synchrogram in Figure 7. The Q output of the one shot U12 pin 10 resets the send flop thereby enabling either flop to be activated at the next positive going transition of the clock.

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SECTION 8

CIRCUIT DESCRIPTION OF THE NOVA INTERFACE

Figure 4 illustrates a UART interconnection to the digital bay of the NOVA. The F4702 chip provides the receiver clock which determines the BAUD rate at which the UART will receive characters. The baud rate is jumper selectable. This is seen from the connections brought out from the 4702 chip on pins 11, 12, 13, and 14. Suitcase jumpers may be used to select the receiver baud rate.

The heart of the design is the COM 2017 UART chip. The chip will receive a serial ASCII string and convert the string to a parallel output of 8 bits (the number of data bits is determined by jumpers on the chip). The eight bits (D0 to D7) are then connected to the input of multiplexer #2. It is through this multiplexer that the information is read into accumulator zero in the NOVA. Notice that input D7 was left open from the UART. This was purposefully done because the multiplexer input corresponding to this data bit was hardwired low. This supplies the zero parity bit necessary to convert the seven remaining bits to the Data General Basic language decimal equivalent of an ASCII character.

The EIA RS-232C information is received by the MC1489 EIA receiver chip. The receiver chip converts the EIA level signals to TTL level signals for input to the COM 2017 chip. At the very start of the serial character coming out of the MC1489 chip, the D flop, U1, is clocked. The Q output of the D flop is inverted by U2, (12, 13-11) and is fed into the EIA driver Chip, U3. The EIA driver circuit U3 supplies the RTS signal to the EIA RS-232C interface coming into the digital bay UART card. As soon as a character string is received, the RTS flag is dropped by the Q output of the D flop to terminate further transmissions from the ACB interface. This handshake method is needed to insure proper reception of all characters.

Upon complete reception of a character the COM 2017 chip will raise the RDA flag which feeds one-half the U2 nand gate (pin 1). With a true on pin 1 the next done flag strobe (DNCHK) coming into pin 2 on U2 will cause U2 pin 3 to send a done flag coming from device 67. This is the signal the software needs before the data is strobed into accumulator zero (ACO) (See Figure 3). After this has been accomplished, a reset pulse (UARS) is sent by the software to reset the RDA flag and the D flop. This is accomplished by sending a low pulse to the "Read Data Available Reset" (RDAR) input on the UART chip. The reset pulse causes the D flop's Output to be low and raises the RTS flag from U3.

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This signals the ACB interface that the digital bay UART is ready to receive another character.

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It is advised at system startup that a UARS pulse be sent to the digital bay UART to insure the integrity of the first character read from the UART. If a call 40 is issued to reset the UART, it will stay in the call if no character was present. And an escape must be pressed to get out of the CALL 40.

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COST AND FABRICATION

Cost of the ACB interface, less labor, is approximately \$300. Approximately 45 man hours are needed for construction and testing of the ACB interface. Table 1 is a list of all parts used in the interface. A printed circuit (PC) card is currently being designed and will probably be available by 6/80. A 9" x 8" Vector board (0.1 x 0.1 inch spacings) was used in conjunction with wirewrap sockets to construct the first prototype. A parts layout is shown in Figure 8.

The memory card for the ACB interface was constructed on a 44 pin Vector plug board, model number 3662-5 for an approximate cost of \$30, less labor. Approximately five man hours are needed for construction and testing of the memory card. The memory card was fabricated separately from the motherboard. This allows more memory to be added to the system with major modifications made only to the memory card. Minor circuit changes are required by the motherboard for memory increments up to 4000 words. A parts layout for the memory board is shown in Figure 9. Table 2 contains a parts list for the memory card.

Cost of the hardware module of the NOVA interface is approximately \$50, less labor. Approximately 15 man hours are needed for construction and testing of the interface. A PC card is currently under design and will probably be available 6/80. The original prototype was constructed on a 44 pin Vector plug board, model number 3662-5, for insertion into the digital interface bay on the NOVA computer. A parts layout for the NOVA interface is shown in Figure 10, and Table 3 contains a parts list for the NOVA interface.

The enclosure and a parts list of the housing are shown in Table 4. Approximately one hour machine shop time was required for front and rear panel drilling and machining. Wiring of the enclosure required approximately three man hours. Cost of the enclosure and parts was included in the original \$300 price for the ACB interface.

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Ryan, D.P., J.M. Teuschler and W.L. Budde. Functional Specifications for the Automation of Flameless Atomic Absorption Spectrophotometers. EPA report to be published, U.S. Environmental Protection Agency, Cincinnati, Ohio.

Budde, W.L., B.P. Almich and J.M. Teuschler. The Status of the EPA Laboratory Automation Project. EPA-600/4-77-025, U.S. Environmental Protection Agency, Cincinnati, Ohio, 1977.

Taber, L., H.S. Ames, R.K. Yamanchi, and G.W. Barton, Jr.. Instrument Calls and Real-Time Code for Laboratory Automation. UCRL-52392, Lawrence Livermore Laboratory, Livermore, California, 1978.

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EPA Form 2850-4 (4-80)

(PREVIOUSLY EPN EPA FORM 881)

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TABLE 1. PARTS LIST FOR ACB INTERFACE (MOTHERBOARD)

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Quan.	Part	Description
1	U1	MC4013B Dual Type D Flip Flop
1	U2	MC4040B 12 Bit Binary Counter
4	U3-U6	MC4503B Hex Noninverting 3 State Buffer
4	U7-U10	MC4049B Hex Inverter/Buffer
1	U11	MC4081B Quad 2 Input AND Gate
1	U12	MC4528B Dual Monostable Multivibrator
3	U13-U15	MC4585B 4 Bit Magnitude Comparator
1	U16	MC4011B Quad 2 Input Nand Gate
1	U17	MC4040B 12 Bit Binary Counter
1	U18	F4702 Programmable Bit Rate Generator
1	U19	MC1489 Quad Line Receiver
1	U20	9616 Triple EIA RS232-C/Mil Std-188C Line Driver
1	U21	F7912UC 3 Terminal Negative 12 Volt Regulator
1	U22	Com 2017 Universal Asynchronous Receiver/Transmitter
20	R1-R20	470 10% 1/4W Carbon Resistor
1	R21	1K 10% 1/4W Carbon Resistor
2	R22-R23	10K 10% 1/4W Carbon Resistor
1	R24	10M 10% 1/4W Carbon Resistor
2	C1-C2	100 pf MICA Capacitor
2	C3-C4	47 pf MICA Capacitor
2	C5-C6	10 µf 25V CDE Capacitor
10		Sprague By Pass Capacitors CKR05BX103KL
1		Crystek CYZB 2.4576MHZ Crystal
4		Scambe 12 Pin Wire Wrap Strips ME-25-C-12-WE B-10
5		Scambe 14 Pin Wire Wrap Socket ME-2B-14-W-G-B-10
15		Scambe 16 Pin Wire Wrap Socket ME-2B-16-W-G-B-10
1		Scambe 24 Pin Wire Wrap Socket ME-2B-24-W-G-B-10
1		Cambion 40 Pin Wire Wrap Socket 703-3885-01-03-16
1		3M 10 Pin Right Angle Wrap Tail Header 3491-3005
1		3M 10 Pin Wrap Tail Mate 3473-7000
1		3M 10 Pin Strain Relief for Wrap Tail Mate 3448-3010
1		3M 24 Pin Wrap Tail Header 3460-0000
1		Vector Board 169P79 Hole Pattern P
34		Vector T49A Wrap Posts
1		TRW Cinch Connectors 50-44-F-10

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TABLE 2. PARTS LIST FOR ACB INTERFACE (MEMORY CARD)

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Quan.	Part	Description
8	U1-U-8	2102A 1K x 1 Bit Static Random Access Memory
1	C1	10 μ f 25V CDE Capacitor
8		Sprague By Pass Capacitors CKR05BX103KL
8		Scambe 16 Pin Wrap Tail Socket ME-2B-16-W-G-B-10
1		Vector Board 3662-5
34		Vector T49A Wrap Posts

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TABLE 3. PARTS LIST FOR NOVA INTERFACE

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Quan.	Part	Description
1	U1	7474 Dual Type D Flip Flops
1	U2	7400 Quad 2 Input Nand Gate
1	U3	9616 Triple EIA RS232-C/Mil Std-188C Line Driver
1	U4	F7912 UC 3 Terminal Negative 12 Volt Regulator
1	U5	MC1489 Quad Line Driver
1	U6	COM 2017 Universal Asynchronous Receiver/Transmitter
1	R1	10 M 10% 1/4W Carbon Resistor
1	R2	1K 10% 1/4W Carbon Resistor
2	R3-R4	1.5 K 10% 1/4W Carbon Resistor
2	C1-C2	47 pf MICA Capacitor
2	C3-C4	10 μ f 25V CDE Capacitor
7		Sprague By Pass Capacitors CKR05BX103KL
1		Crystek CYZB 2.4576MHZ Crystal
4		Scambe 14 pin Soldier Tail Socket US-Z-14-110-G-B
1		Scambe 16 pin Soldier Tail Socket US-Z-16-110-G-B
1		Scambe 40 pin Soldier Tail Socket US-2-40-110-G-B
1		Vector Board 3662-5

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TABLE 4. PARTS LIST FOR ACB INTERFACE (ENCLOSURE)

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Quan.	Description
1	Designer II 52-3-10 Black Interface Box
1	LAC3GD Switchcraft AC Receptacle
1	Littelfuse 342012A 10A 250V Fuse Holder
1	iPi Power Switch Type 416
1	Semiconductor Circuits Power Supply MP 1.5.500/2.15.100
1	Semiconductor Circuits Power Supply Plate 46-0005-22
1	Beldon 3 Conductor Power Supply Cord 179525
2	TRW Cinch Connectors DB 255
23	Led's Fairchild FLV-260 Red Diffused
23	Led Mounting Hardware Fairchild FL5011
18"	3M Scotchflex Flat Cable 3302-26 Conductor

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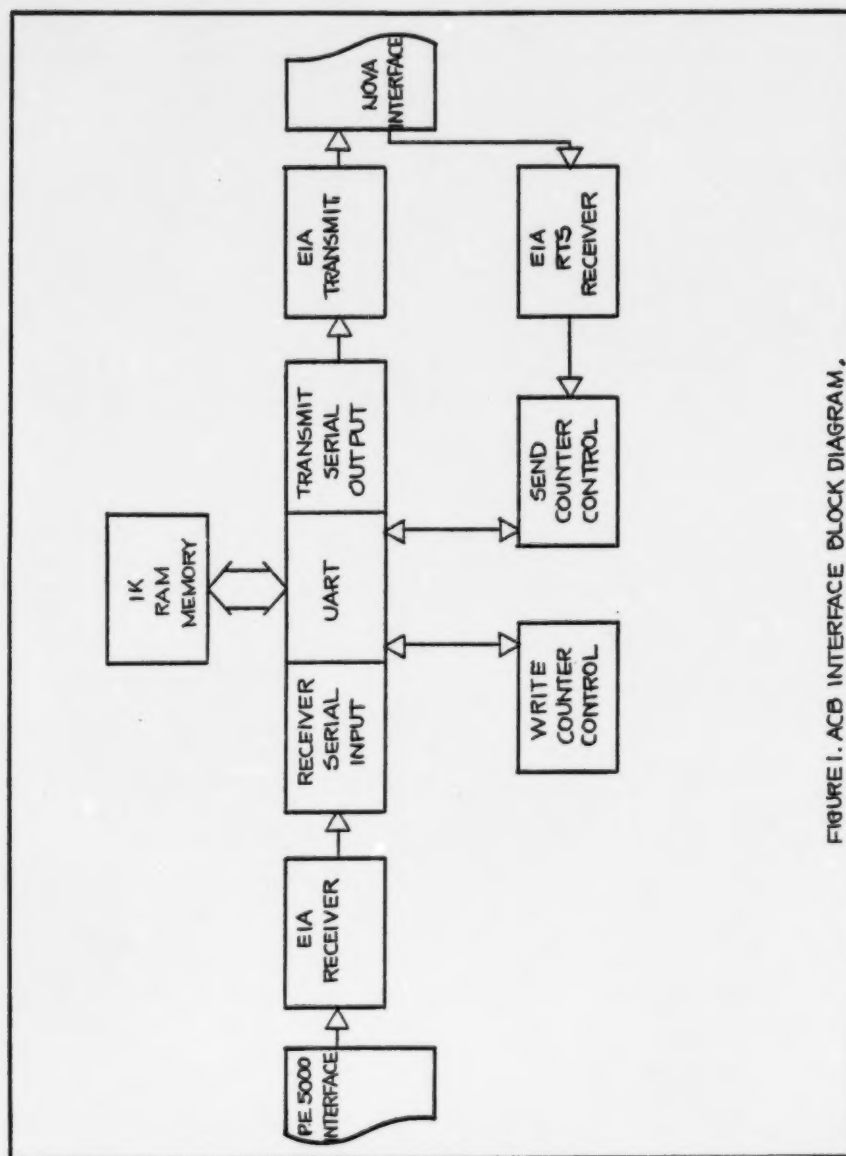


FIGURE 1. ACB INTERFACE BLOCK DIAGRAM.

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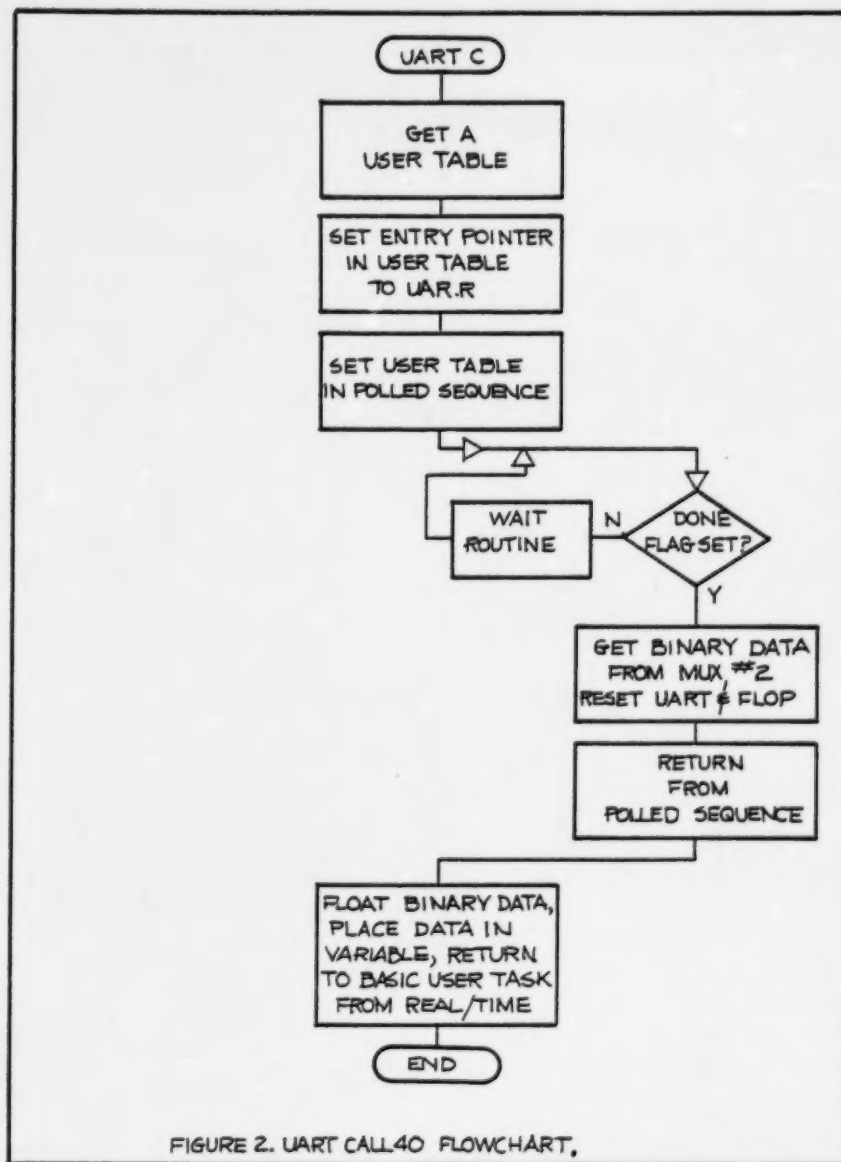


FIGURE 2. UART CALL40 FLOWCHART.

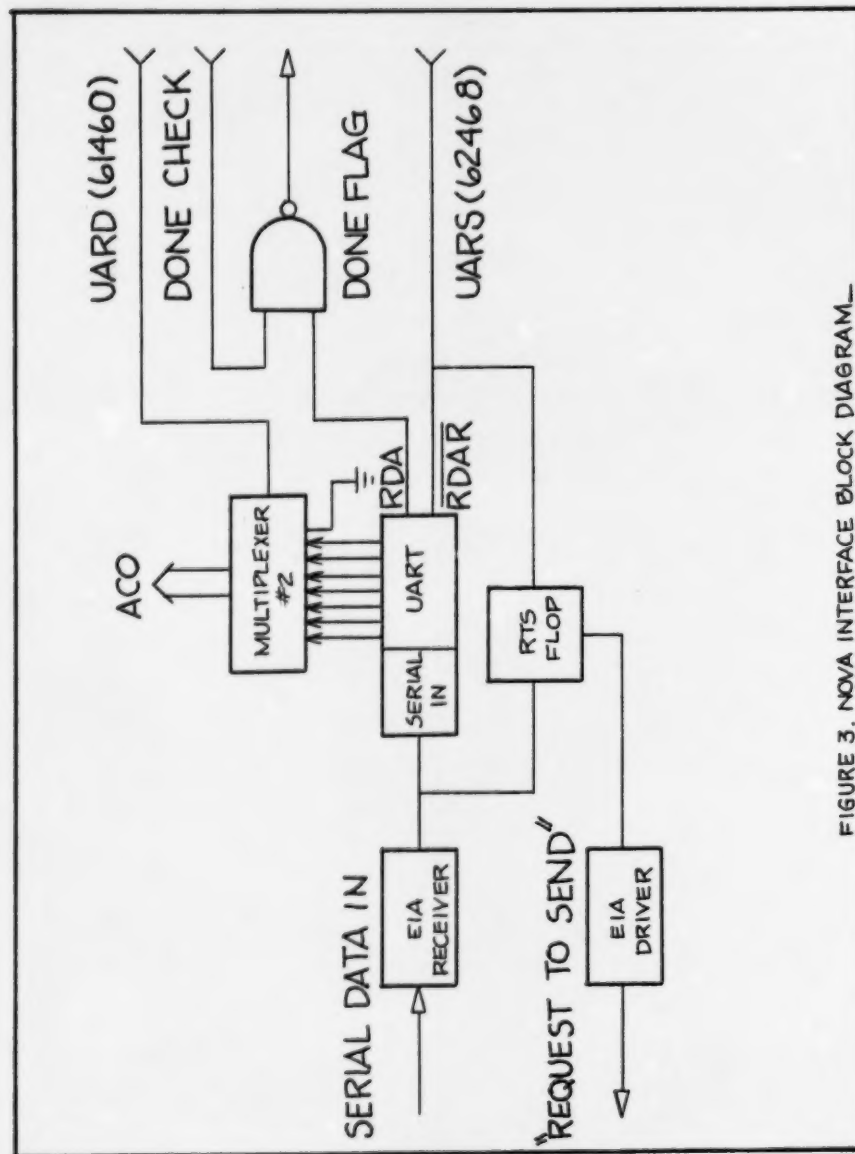


FIGURE 3. NOVA INTERFACE BLOCK DIAGRAM

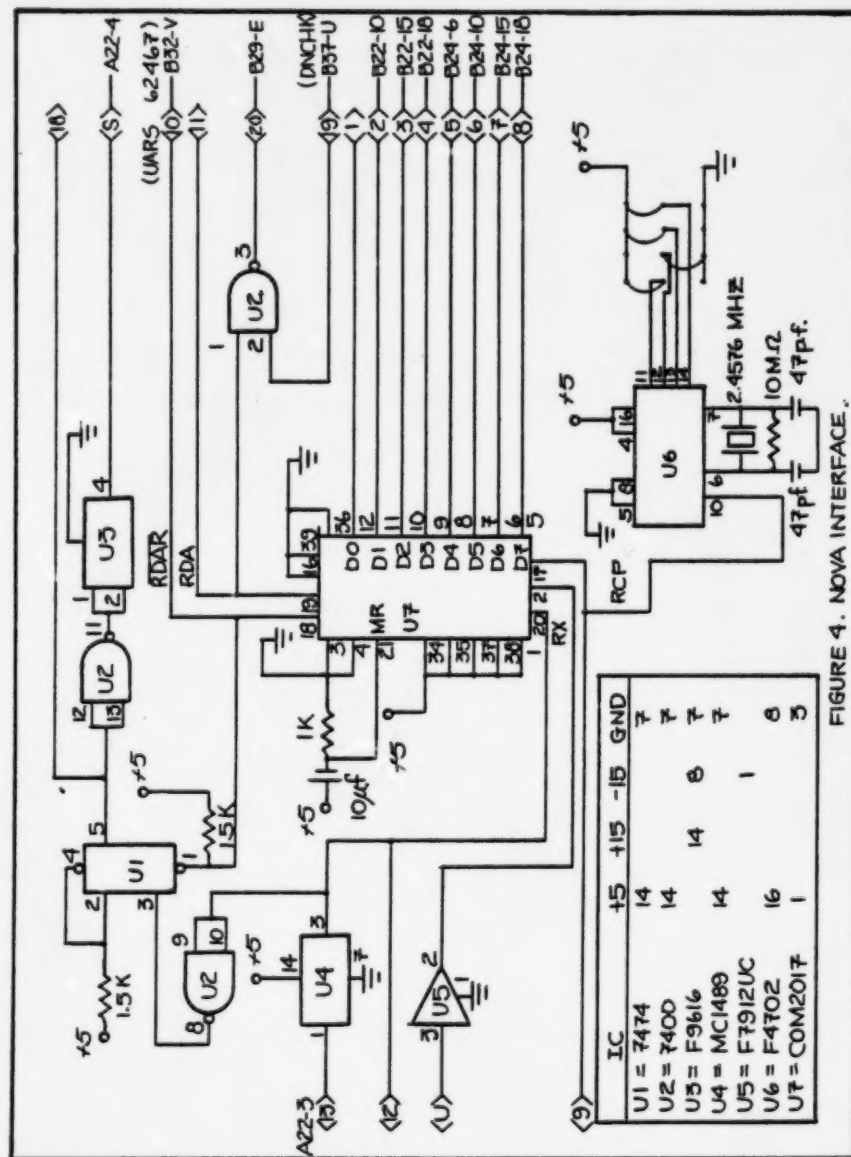


FIGURE 4. NOVA INTERFACE.

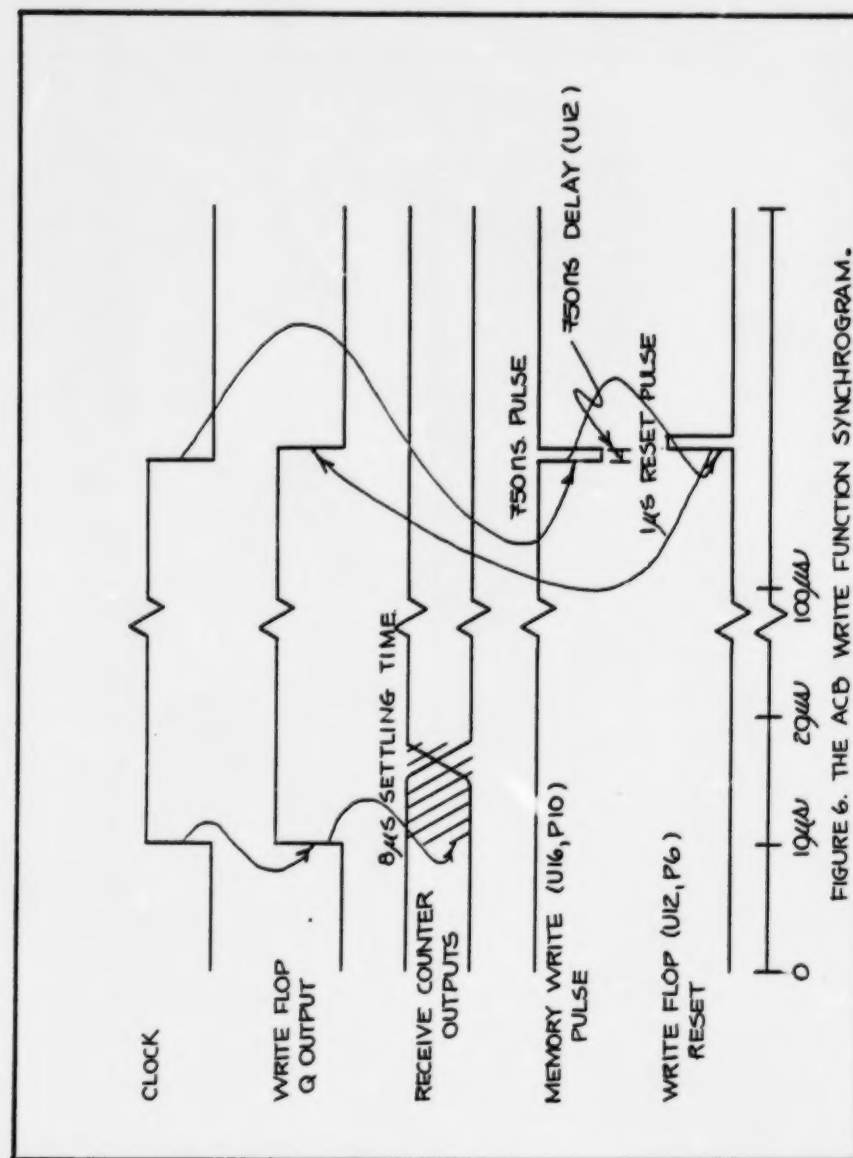


FIGURE 6. THE ACB WRITE FUNCTION SYNCHROGRAM.

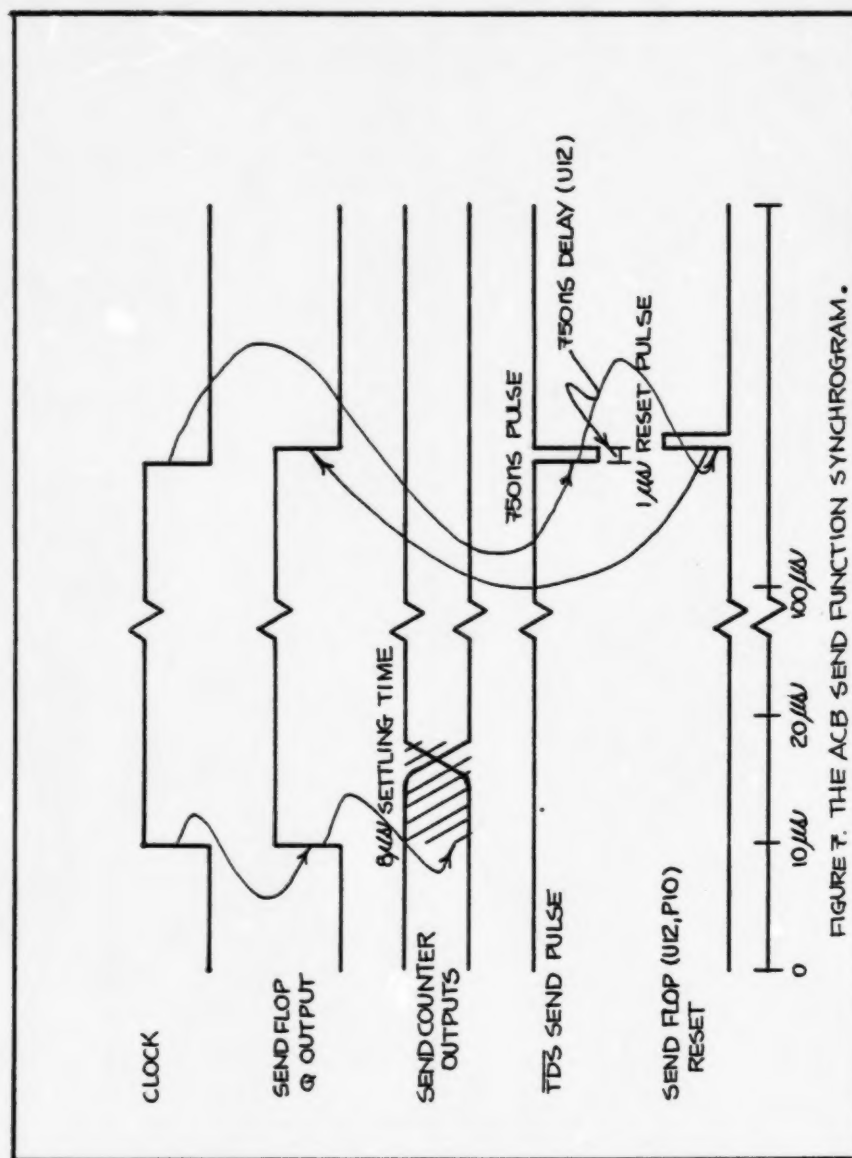


FIGURE 7. THE ACB SEND FUNCTION SYNCHROGRAM.

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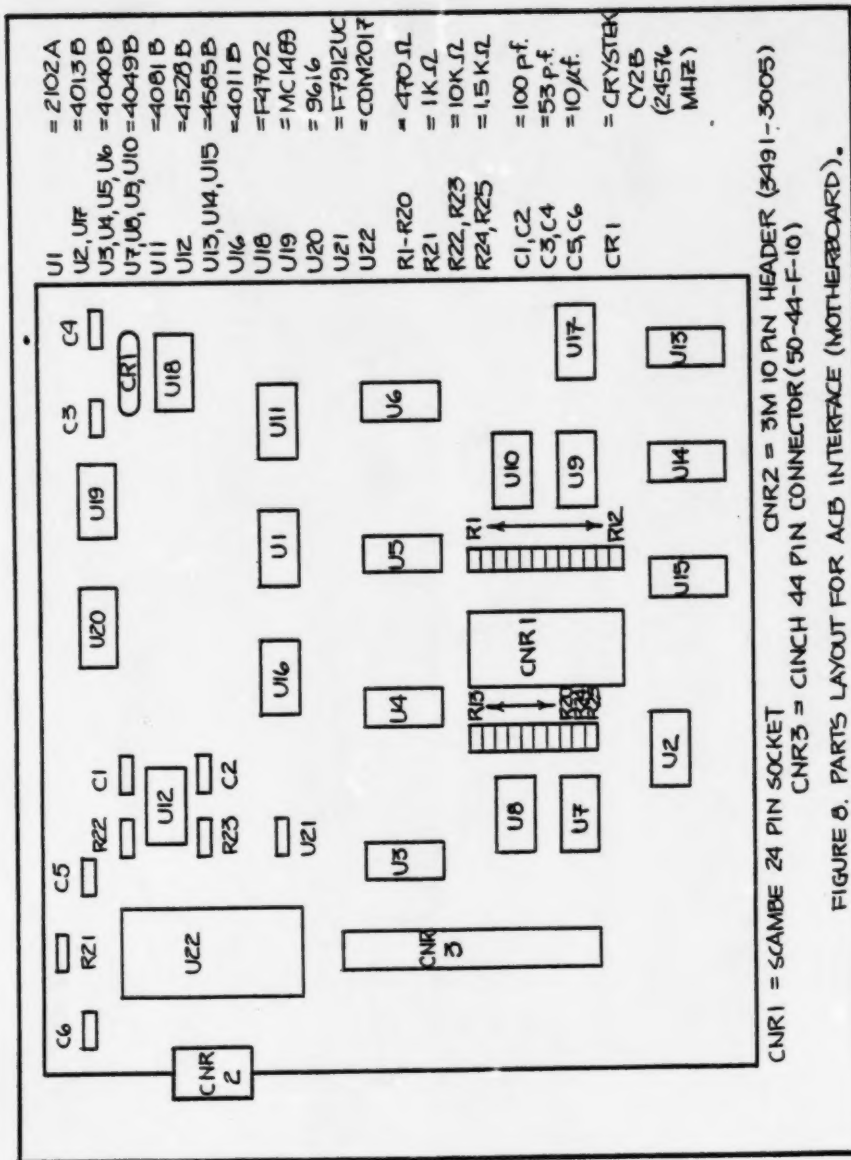


FIGURE 8. PARTS LAYOUT FOR ACB INTERFACE (MOTHERBOARD).

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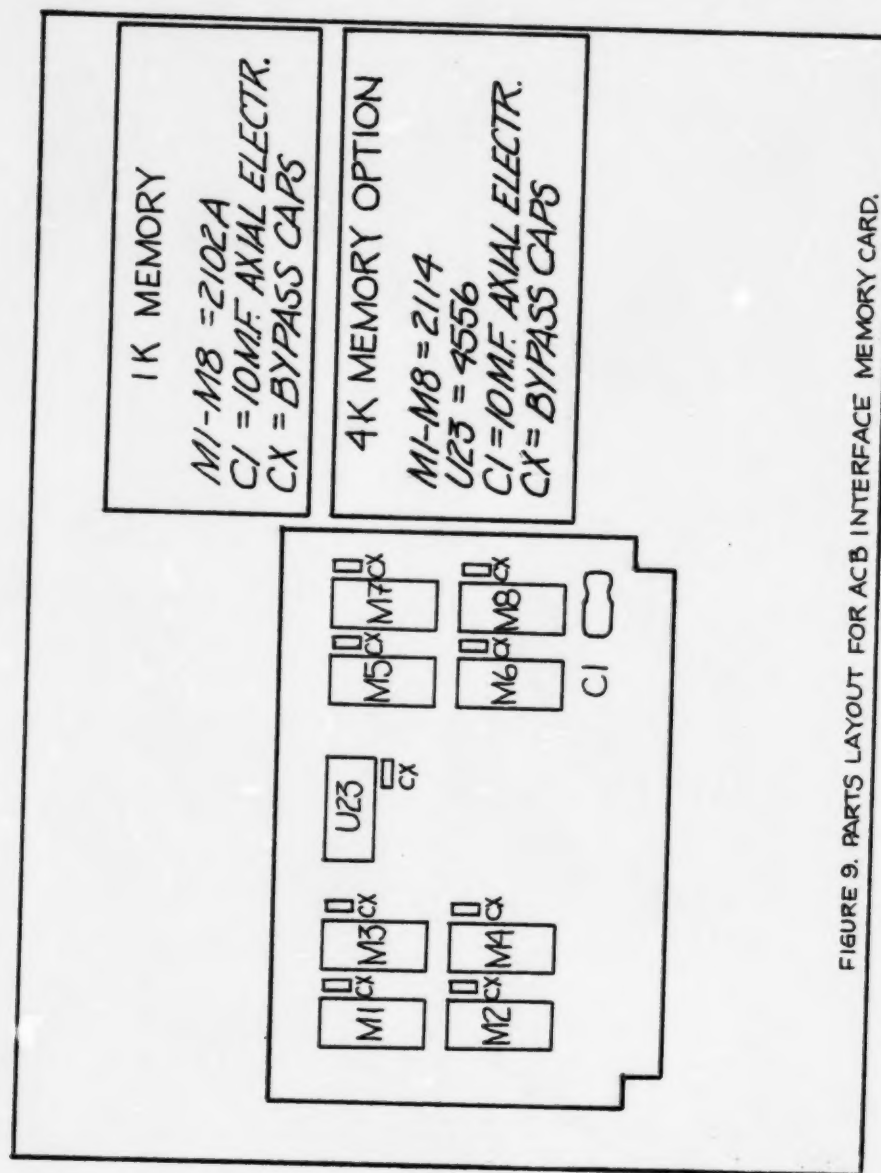


FIGURE 9. PARTS LAYOUT FOR ACB INTERFACE MEMORY CARD.

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C1, C2 = MICA 47 P.F.
C3 = ELECTRO. 10 M.F.
C4 = AXIAL ELECT. 10 M.F.
CX = BYPASS CAPS
CR1 = CRYSTEK CY2B
24576 MHZ.
R1 = 10 M Ω
R2 = 1 K Ω
R3, R4 = 1.5 K Ω

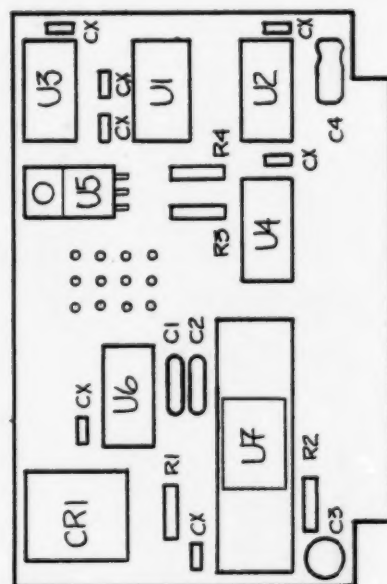


FIGURE 10. PARTS LAYOUT FOR NOVA INTERFACE.

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APPENDIX A

EIA MODEM-TERMINAL INTERFACE

PIN	NAME	TO DTE	TO DCE	FUNCTION	CIRCUIT CCITT	(EIA)
1	FG			FRAME GROUND (NO SWITCH).....	101	(AA)
2	TD		-	TRANSMITTED DATA.....	103	(BA)
3	RD	-		RECEIVED DATA.....	104	(BB)
4	RTS		-	REQUEST TO SEND.....	105	(CA)
5	CTS	-		CLEAR TO SEND.....	106	(CB)
6	DSR	-	6-1/2"	DATA SET READY.....	107	(CC)
7	SG			SIGNAL GROUND.....	102	(AB)
8	DCD	-		DATA CARRIER DETECT.....	109	(CF)
9		-		POSITIVE DC TEST VOLTAGE		
10		-		NEGATIVE DC TEST VOLTAGE		
11	QM	-		EQUALIZER MODE.....	BELL	208A
12	(S)DCD	-		SEC. DATA CARRIER DETECT.....	122	(SCF)
13	(S)CTS	-		SEC. CLEAR TO SEND.....	121	(SCB)
14	(S)TD		-	SEC. TRANSMITTED DATA.....	118	(SBA)
	NS		-	NEW SYNC.....	BELL	208A
15	TC	-		TRANSMITTED CLOCK.....	114	(DB)
16	(S)RD	-		SEC. RECEIVED DATA.....	119	(SBB)
	DCT	-		DIVIDED CLOCK TRANSMITTER.....	BELL	208A
17	RC	-		RECEIVER CLOCK.....	115	(DD)
18	DCR	-		DIVIDED CLOCK RECEIVER.....	BELL	208A
19	(S)RTS		-	SEC. REQUEST TO SEND.....	120	(SCA)
20	DTR		-	DATA TERMINAL READY.....	108.2	(CD)
21	SQ	-		SIGNAL QUALITY DETECT.....	110	(CG)
22	RI	-		RING INDICATOR.....	125	(CE)
23			-	DATA RATE SELECTOR.....	111	(CH)
			-	DATE RATE SELECTOR.....	112	(C)
24	(TC)		-	EXT. TRANSMITTER CLOCK.....	113	(DA)
25			-	BUSY.....	BELL	1138

- POSITIVE VOLTAGE EQUALS BINARY ZERO, SIGNAL SPACE, CONTROL ON
- NEGATIVE VOLTAGE EQUALS BINARY ONE, SIGNAL MARK, CONTROL OFF

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APPENDIX B

PERKIN ELMER 5000 EIA-RS-232C INTERFACE DESCRIPTION

The circuits provided by the interface at the 25-pin RS-232C/TTY accessory connector are as follows:

From To Model 5000	Pin	RS-232C Circuit	Function
←---	1	AA	Protective Ground
---→	2	BA	Transmitted Data
←---	3	BB	Received Data
←---	5	CB	Clear to Send
←---	6	CC	Data Set Ready
←---	7	AB	Signal Ground
←---	8	CF	Data Carrier Detect

Circuits CB, CC and CF (Pins 5,6 and 8) are held to EIA ON when instrument power is on.

Rev. October 1978

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APPENDIX C ASSEMBLY CODE INTERFACE TO THE NOVA

The following code is used to implement a call 40 in the basic language it was written by J. Teuschler in the latter part of 1979. It checks a UART in the digital bay for a RDA flag. If RDA is true, a character is returned in the variable of the Call 40. When the character is read from the UART, the UART is automatically reset so another character can be received by the UART.

```

.TITLE      UART ;DIGITAL BAY UART DRIVER
.NREL
.DUSR      SIXSEV= 67 ;DEVICE CODE OF UART DONE FLAG
.DUSR      UARS= 62467 ;UART RESET (RESETS RDAR AND DONE FLOP)
.DUSR      UARD= 61460 ;UART READ (CHANNEL 2 MUX STROBE)
.ENT       UARTC ;CALL ENTRY FROM SBRTB. SR
.EXTD      C3 ;JUST A CONSTANT
.EXTD      .TABL ;SUB TO ASSIGN A TABLE
.EXTD      .FLOT ;SUB TO FLOAT A NUMBER
.EXTD      TR3 TR4
.EXTN      ES. W ES.V ;SUB TO WAIT
.EXTN      . RECS ; REC WITH SWAPPING
.EXTN      NEXTL ;LINK TO NEXT R/T TABLE
.EXTN      FRRT ;RETURN FROM REAL TIME
UARTC: JSR@ .TABL ;GET A TABLE
LDA 0.UARR ;POINTER TO R/T ROUTINE
STA 0,1,2, ;R/T ENTRY POINT
RT. GO ;R/T GO OBVIOUSLY
LDA 2,TR4 ;GET THE R/T TABLE
LDA 1,5,2 ;GET THE BINARY #
ZERO 0 ;ZERO AC 0
JSR@ .FLOT ;FLOAT IT
JMP .+1 ;NOT MUCH OF AN ERROR RETURN
LDA 3,TR3 ;STAIRWAY TO BASIC
LDA 2,0,3
FLS 2
JMP 1,3 ;BRING BASIC USER TASK BACK

DFRRT: FRRT
U10: 10 ;10/60 THS OF A SECOND
UARR: UAR.R ;POINTER TO UAR. R
UARTV: ES. V ;WAIT POINTER
UARWW: ES. W ;WAIT ENTRY
UAR. R: LDA 1,UARTV ;ENTRY POINTER = WAIT ROUTINE
STA 1,4,2 ;WAIT SUB IS NOW R/T ENTRY POINT

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DNCHK:	SKPDN	SIXSEV	;DONE FLAG SET ON DEV 67?
	JMP	UARTW	;NOPE- GO WAIT
	UARD		;YEP, MUX THE DATA IN
	STA	0,5,2	;STORE BINARY DATA IN POS 5 OF R/T TABLE
	UARS		;RESET UART SO ANOTHER CHARACTER CAN BE RECEIVED
	JMP@	DFRRT	;RETURN FROM POLLING
UARTW:	LDA	1,U10	;GO DO THE WAIT SCENE
	JSR@	UARWW	;OFF TO THE WAIT ROUTINE
	JMP	DNCHK	;CHECK THE DONE FLAG AGAIN

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